"RESPONSE UNDER 37 CFR 1.116-
EXPEDITED PROCEDURE EXAMINING
GROUP 2816 "

206569US

#13 (3rd)

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF: :

KOICHI MOTOIKE : EXAMINER: WELLS, KENNETH B 2/11/03

SERIAL NO. : 09/841,595 :

FILED: APRIL 25, 2001 : GROUP ART UNIT: 2816

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT :

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AMENDMENT UNDER 37 CFR §1.116

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

will not be entered /cm 2/11/03

SIR:

In response to the Official Action dated November 5, 2002, please amend the above-identified patent application as follows:

IN THE CLAIMS

Please amend Claims 1 and 11 as shown in clean form below. A marked-up copy of amended Claims 1 and 11 is attached.

C1

1. (Twice Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal with a predetermined frequency and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal of said FET and a ground terminal, said inductor element having an inductance value selected in accordance with the predetermined frequency of said controlled signal and forming a